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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/051,541	01/16/2002	Mark Champion	71746	9648

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EXAMINER	
MONESTIME, MACKLY	

ART UNIT	PAPER NUMBER
2676	3

DATE MAILED: 11/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

KS

Office Action Summary	Application No.	Applicant(s)	
	10/051,541	CHAMPION, MARK	
	Examiner	Art Unit	
	Mackly Monestime	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *21-28* is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-27 are presented for examination.

Specification

2. Applicant is requested to update the related applications information in the specification. Update with serial number or patent number (page 1, lines 24-25).

Drawings

3. Figures 1A-1B; Fig. 2; Figs. 3A, 3B, 3C; Fig. 4; Fig. 5; Figs. 6A, 6B and 6C should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Double Patenting

4. Claims 1-18 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-16 of copending application No. 10/051,680. Although the conflicting claims are not identical, they are not in fact patentably distinct from each other because the subject matter claimed in the instant application is substantially disclosed in the referenced copending application and would be covered by any patent granted on that copending

application since the referenced copending application and the instant application are claiming common subject matter, the only difference between claim 1 of application (10/051,680) and claim 1 of copending application (10/051,541) is that the buffer page system of the present application (10/051,541) further comprising: "at least two memory devices, wherein data elements are storedto at least one memory device and retrieve from at least one memory device in parallel". These limitations are added in the present application (10/051,541). However, both claims recite the same combination of elements/steps having the same function. Therefore, one of ordinary skill in the art would have been motivated to incorporate the added limitations (at least two memory devices; wherein data elements can be stored and retrieved in parallel) to the present claims because doing so would not only provide more storage capability that is often required for more complex data processing functions, but also enhance the performance of the system by executing multiple operations (such as storing and retrieving data) simultaneously, thereby enhancing the processing speed of the overall system.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-11,13-17 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art in view of Schlapp et al (US Patent No. 5,579,473).

7. As per claims 1-3, AAPA substantially disclosed the invention as claimed, including a buffer page system, comprising: a data source, providing data elements in a first order (Fig. 4, Item No. 405); a data destination, receiving data elements in a second order (Fig. 4, Item No. 420); at least two memory devices, each memory device having a plurality of memory pages including a plurality of memory locations, each memory location having an address, where data elements are stored to each memory device in the first order and retrieved from each memory device in the second order, and where each memory page stores data elements in multiple locations according to the first order and stores data elements in multiple locations according to the second order (Fig. 4, Items No. 410 and 415; page 5, lines 16-22).

AAPA did not expressly disclose where each data element corresponds to an entry in one of a plurality of buffer pages, each buffer page having a plurality of entries along a first dimension corresponding to the first order and a plurality of entries along a second dimension corresponding to the second order. However, AAPA did disclose a typical frame buffer architecture 400 capable of accessing pixel data for two pixels in parallel (page 5, lines 16-17); AAPA further disclosed a typical frame buffer architectures often also utilize "double-buffering", where the memory address space of a frame buffer is divided into two sections; wherein, in some architectures, each section is a separate memory device, and in other architectures one or more devices are each divided into sections. Data from a frame is stored in one section while data from a previously stored frame is

read from the other section (page 8, lines 2-8). Moreover, Schlapp et al disclosed a set of four DRAM banks (DRAM banks A-D) and corresponding page buffers A-D, wherein, each DRAM bank A-D comprises a 2.5 megabit DRAM array arranged in 257 pages (col. 4, lines 42-45). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have incorporated the plurality of buffer pages taught by Schlapp et al into the teachings of AAPA because doing so would allow the buffer controller to access page operations to one of the DRAM banks A-D with rendering operations into another of the DRAM banks A-D.

8. As per claim 4, AAPA disclosed a data element is pixel data corresponding to a pixel in a frame of pixels, the frame having horizontal rows of pixels and vertical columns of pixels (page 3, lines 22-26); AAPA furthe disclosed that a grid of pixel 110, wherein the pixels 110 are often number sequentially for reference with pixel 0 typicallyat the upper left (page 3, lines 29-31).

9. As per claim 5, AAPA disclosed each row of the frame includes 1920 pixels and each column of the frame includes 1080 pixels (HD resolution; page 3, lines 27-28).

10. As per claims 6-10, AAPA disclosed that the typical frame buffer is being able to access pixel data for two pixels in parallel in which pixel data are stored and retrieved from the first and second memory (Fig. 4, Items No. 410 and 415) and to operate based on clock cycles such that two pixels are processed per clock cycle (page 5, lines 16-22; page 6, lines 8-10).

11. As per claim 11, AAPA disclosed where pixel data is stored at a rate supporting 60 frames per second, and pixel data is retrieved at a rate supporting 120 frames per second (page 4, lines 17-30).

12. As per claim 13, AAPA disclosed memory devices SDRAM operate at approximately 150MHz (Page 5, line 3); but did not explicitly disclose that each memory device is an 8 MB. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have included memories having 8 MB in order to provide more storage capabilities for high resolution images.

13. As per claim 14, AAPA disclosed a memory controller for generating addresses for storing and retrieving data elements (Fig. 5, Item No. 545).

14. As per claims 15-17, AAPA disclosed that the video source provides pixel data for a first pixel to a first data bus (first state) and pixel data for a second pixel to a second data bus such that the first memory stores the pixel data on the first data bus at the address supplied by the memory controller or multiplexer from the video source and the second memory stores the pixel data on the second data bus at the same address (second state; page 6, lines 26-29; page 7, lines 16-26).

AAPA did not disclosed four memory devices. However, Schlapp et al disclosed a set of four DRAM banks (DRAM banks A-D) and corresponding page buffers A-D, wherein, each DRAM bank A-D comprises a 2.5 megabit DRAM array arranged in 257 pages (col. 4, lines 42-45). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references because doing so would not only provide more storage

capability that is often required for more complex data processing functions, but also enhance the performance of the system by executing multiple operations simultaneously, thereby enhancing the processing speed of the overall system.

15. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art in view of Schlapp et al as applied to claims 1-11 above, in further in view of " Alternative Architecture for High Performance Display" by R.W. Corrigan et al.

16. An Alternative Architecture for High Performance Display" by R.W. Corrigan et al. was cited in IDS#2.

17. As per claim 12, AAPA did not explicitly disclose that pixel data is retrieved for 64 pixels for every 32 pixels of pixel data that is stored; thus AAPA did disclose that pixel rates vary among implementations (Fig. 2). However, Corrigan et al disclosed that the frame buffer usually reads and refreshes the display up to four times the input rates. Moreover, since the resolution and detail of the image are largely determined by the number of pixels in the frame buffer. Therefore, one of ordinary skill in the art would have been motivated to combine the cited references because doing so provide better resolution and higher image quality.

18. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art in view of Schlapp et al as applied to claims 1-11, 14-17 above, and further in view of Goodwin et al (US Patent No. 6,226,709).

19. As per claim 18, the combination did not disclose a four by four switch providing data elements to the four memories. However, Goodman et al disclosed a cross-bar switch connects up

to four memory modules, each comprising up to eight interleaved memory ranks (col. 3, lines 54-57). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references because doing so would improve system's flexibility.

20. As per claim 19, AAPA substantially disclosed the invention as claimed, including a pixel page system comprising: a video source providing pixel data for pixels in a frame, the frame having rows of pixels and columns of pixels (page 3, lines 24-26); a video destination (Fig. 5, Item No. 520); a first memory having a plurality of memory locations (Fig. 5, Item No. 510); a second memory having a plurality of memory locations (Fig. 5, Item No. 515); a memory controller connected to the first memory and the second memory (Fig. 5, Item No. 545); a first data bus connected to the memory controller ; a second data bus connected to the memory controller (Fig. 5, Items No. 525, 530); a source address line connected to the video source and the memory controller (Fig. 5, Item No. 535); a destination address line connected to the video destination and the memory controller (Fig. 5, Item No. 550); and where each pixel corresponds to an entry in one of a plurality of pixel pages, and a pixel page includes multiple pixels from a row in the frame and multiple pixels from a column in the frame, and each pixel page includes at least one pixel in the frame, and where each entry in a pixel page corresponds to a memory location (page 6, lines 11-19).

AAPA did not disclosed four memory devices. However, Schlapp et al disclosed a set of four DRAM banks (DRAM banks A-D) and corresponding page buffers A-D, wherein, each DRAM bank A-D comprises a 2.5 megabit DRAM array arranged in 257 pages (col. 4, lines 42-

45). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references because doing so would not only provide more storage capability that is often required for more complex data processing functions, but also enhance the performance of the system by executing multiple operations simultaneously, thereby enhancing the processing speed of the overall system.

21. As per claim 20, AAPA disclosed that the memory controller generates addresses for storing and retrieving pixel data (page 7, lines 17-21).

Allowable Subject Matter

22. Claims 21-28 are allowable over the prior art of record.

23. The prior art of record further failed to teach or render obvious the combination of elements recited in the claim. The cited references did not specifically disclose or suggest the following limitations: " a first address multiplexor connected to the first memory; a second address multiplexor connected to the second memory; a third address multiplexor connected to the third memory; a fourth address multiplexor connected to the fourth memory; a four-by-four switch connected to the first memory, the second memory, the third memory, and the fourth memory, having a first data input, a second data input, a first data output and a second data output, where the four-by-four switch switches with each frame between providing pixel data to the first memory and the second memory while receiving pixel data from the third memory and the fourth memory, and receiving pixel data from the first memory and the second memory while

providing pixel data to the third memory and the fourth memory (as per claim 21)". These distinct structure of the present claims invention were not found to be anticipated, suggested or made obvious by the prior art of record, either singularly or in combination.

24. The prior art of record further failed to teach or render obvious the combination of elements recited in the claim. The cited references did not specifically disclose or suggest the following limitations: " storing pixel data for a first and second frame of pixels in a first and second memory using pixel pages, wherein at least one memory page stores pixel data for at least two pixel two pixels from each of at least two horizontal rows of pixels in the first and second frame of pixels" (as per claim 23 and 27). The above limitations of the present claims invention were not found to be anticipated, suggested or made obvious by the prior art of record, either singularly or in combination.

Conclusion

Applicant is required to give full consideration to these prior art references when responding to this office action.

The prior arts made of record and not relied upon is considered pertinent to applicant's disclosure.

Baker et al (US Patent No. 6,347,344) taught an integrated multimedia system with local processor, data transfer switch, processing modules, fixed functional unit, data streamer, interface unit and multiplexer all integrated on multimedia processor.

Yamamoto et al (US Patent No. 5,798,843) taught an image processing system with a buffer memory.

Schiefer et al (US patent No. 6,177,922) taught a multi-scan video timing generator for format conversion.

Saitoh (US Patent No. 5,479,605) taught a raster scan operation apparatus for executing a drawing arithmetic operation when window are displayed.

Rivshin (US Patent No. 5,303,341) taught a video processor for a printing apparatus.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mackly Monestime whose telephone number is (703) 305-3855. The examiner can normally be reached on Monday to Thursday from 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bella Matthew, can be reached on (703) 308-6829.

Any response to this action should be mailed to:

Commissioner of Patent and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, Va, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Mackay Monestime

Patent Examiner

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

October 30, 2003